IN THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) A transmitter circuit means comprising:

a phase lock loop including a phase detector means, a summation means, and a voltage controlled oscillator arranged in series, and a controllable frequency divider arranged to feedback an output of the voltage controlled oscillator to an input of the phase detector; and

a baseband modulation source arranged to generate a modulation signal corresponding to information to be transmitted;

a modulation correlation circuit means arranged to receive said modulation signal and to correlate said signal with residual modulation in the phase lock loop to generate one or more modulation correction signals;

a delta-sigma modulator means arranged to receive said modulation signal and generate a delta-sigma control signal therefrom; and

a modulation amplitude scaling means arranged to receive the modulation signal and the modulation correction ~~signal sand~~ signals and to scale the amplitude of the modulation signal in response thereto;

wherein the scaled modulation signal is applied to the phase lock loop at the summation means in order to modulate the voltage controlled oscillator to produce a modulated RF output signal; and

the delta-sigma control signal is applied to the controllable frequency divider in order to control the divide ratio thereof whereby the controllable frequency divider acts to substantially remove the modulation from the modulated RF output signal at the input to the phase detector.

2. (Previously presented) A transmitter circuit means according to claim 1, further comprising a reference frequency source arranged to generate a reference frequency signal, said phase detector means being arranged to receive said reference frequency signal at a second input and to generate a phase error signal corresponding to the relative phase error between the reference frequency signal and the output RF signal.

3. (Previously presented) A transmitter circuit means according to claim 2, wherein said phase detector means further comprises:

a phase error detection means arranged to detect the relative phases of said reference frequency signal and said output RF signal; and

a charge pump arranged to generate said phase error signal in response to the detected phase error.

4. (Original) A transmitter circuit means according to claim 3, further comprising a charge pump scaling means arranged to control the charge pump to scale the amplitude of the phase error signal generated therein, said charge pump scaling means being responsive to a charge pump correction signal generated by said modulation correlation circuit means.

5. (Previously presented) A transmitter circuit means according to claim 2, further comprising a low pass loop filter arranged to receive said phase error signal, and to output a filtered phase error signal to said summation means as the input to said means.

6. (Previously presented) A transmitter circuit means according to claim 1, and further comprising:

at least one storage means arranged to store a programmable reference multiplier constant P and a programmable fractional frequency offset constant F;

a first adder arranged to stun the modulation signal and the constant F, and output the result to the delta-signal modulator; and a second adder arranged to sum the output of the delta-sigma modulator and the constant P to give the delta-sigma control signal.

7. (Previously presented) A transmitter circuit means according to claim 1, wherein said modulation correlation circuit means further comprises:

a differentiator arranged to receive the phase error signal and to differentiate said signal to give a frequency deviation signal corresponding to the residual modulation in the phase lock loop;

a high pass filter arranged to receive the modulation signal from said baseband modulation source and to filter said modulation signal to remove any low frequency components;

a correlator arranged to receive said frequency deviation signal and said filtered modulation signal, and to output a master control signal; and

control signal generation means arranged to receive said master control signal and to generate at least said modulation correction signals in response thereto.

8. (Original) A transmitter circuit means according to claim 7, wherein said control signal generation means also generates said charge jump correction signal in response to said master control signal.

9. (Previously presented) A transmitter circuit means according to claim 7, wherein said modulation correlation circuit means further comprises:

a delay means arranged to apply a 1-bit delay to said modulation signal output from said baseband modulation source prior to being fed to said high pass filter; and

a switch means arranged between said correlator and said control signal generation means, said switch means being further arranged to be operable in response to a reversal signal output from said baseband modulation source, wherein said switch means opens when said reversal signal indicates that a bit repeat has occurred and closes when said reversal signal indicates that a bit reversal has occurred.

10. (Previously presented) A transmitter circuit means according to claim 7, wherein said modulation correlation circuit further comprises a delay means arranged to apply a 1-bit delay to said modulation signal output from said baseband modulation source means prior to being fed to said high pass filter;

a first switch means arranged between said phase detector means and said differentiator, and

a second switch means arranged between the output of said delay means and the input of said high pass filter,

wherein said first and second switch means are further arranged to be operable in response to a reversal signal output from said baseband modulation source, wherein said first and second switch means open when said reversal signal indicates that a bit repeat has occurred and closes when said reversal signal indicates that a bit reversal has occurred.

11. (Currently amended) A transmitter circuit means according to claim 7, wherein said modulation correlation circuit means further comprises a low pass filter arranged between the output of said ~~differenriator~~ differentiator and the input of said correlator to low pass filter said frequency deviation signal.

12. (Previously presented) A transmitter circuit means according to claim 7, wherein said modulation correlation circuit comprises a second low pass filter arranged at the input to said control signal generation means, to low pass filter said master control signal.

13. (Previously presented) A transmitter circuit means according to claim 7, wherein said control signal generation means comprises:

a first comparator arranged to compare the master control signal with a reference value a, and to output a fast result signal when said master control signal is greater than (+a);

a second comparator arranged to compare the master control signal with said reference value a, and to output a second result signal when said master control signal is less than (-a);

a counter arranged to be decremented in response to said first result signal and to be incremented in response to said second result signal; and

a digital to analogue converter (DAC), arranged to generate an analogue signal representation of the value of said counter;

wherein said modulation correction signal is derived from the analogue output of said DAC.

14. (Original) A transmitter circuit means according to claim 13, wherein said charge pump correction signal is derived from the output of said DAC.

15. (Previously presented) A transmitter circuit means according to any of claim 7, wherein said high pass filter, said low pass filter, and said second low pass filter are each any one of a digital, analogue, or switched capacitor filter respectively.

16. (Previously presented) A transmitter circuit means according to claim 1 wherein said transmitter circuit means provides a phase modulated output.

17. (CANCELLED)

18. (Previously presented) A method for generating a modulated RF output signal in a phase lock loop including a phase detector means, a summation means and a voltage controlled oscillator arranged in series and a controllable frequency divider arranged to feedback an output to the voltage controlled oscillator to an input of the phase detector, the method comprising the steps of:

generating a modulation signal corresponding to information to be transmitted; and characterized by further comprising the steps of:

generating a delta-sigma control signal from the modulation signal in a delta-sigma modulator;

applying the modulation signal to the summation means to modulate the voltage controlled oscillator to produce the modulated RF output signal as the output of said oscillator;

applying the delta-sigma control signal to the controllable frequency divider in order to control the frequency divide ratio thereof;

frequency dividing the modulated RF output signal in the controllable frequency divider in accordance with the frequency divide ratio of the divider;

correlating residual modulation in the phase lock loop with the modulation signal, the result of the correlation being used to generate a modulation correction signal; and

scaling the modulation signal applied to the summation means in response to the modulation correction signal;

wherein said step of frequency dividing substantially removes the modulation from the RF output signal at the input of the phase detector.